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I. REAL PARTY OF INTEREST

According to MPEP § 1206, identification of the real party of interest will allow members of the board to comply with ethic regulations. This application has been assigned to Vishay Dale Electronics, Inc., a Delaware Corporation, having an address of 1122 23rd Street, P.O. Box 609, Columbus, NE, 68602-0609.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences at this time.

III. STATUS OF CLAIMS

Claims 1-5 and 15-16 are pending and appealed. No other claims are currently pending.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF THE INVENTION

The present invention is directed towards a method of manufacturing a thin film chip resistor which includes a tantalum pentoxide moisture barrier (Specification, p. 1, lines 4-6; p. 3, lines 16-20). The moisture barrier reduces failures due to electrolytic corrosion (Specification, p. g, line 12 through p. 6, line 27). The resistive thin film can be any of a

number of materials because the tantalum pentoxide layer is deposited, such as through sputtering. Standard testing of resistors formed from the process indicated great reductions or elimination of failures due to electrolytic corrosion under powered moisture conditions (Specification, P. 5, line 12 through p. 6, line 27). Thus, the present invention recognizes that failures due to electrolytic corrosion under powered moisture conditions of a chip resistor can be reduced or eliminated by depositing an outer layer of tantalum pentoxide. Because the outer layer of tantalum pentoxide is deposited, any of a number of types materials can be used for the resistive element.

VI. ISSUES

1. Did the Examiner improperly combine the multi-component module of Copetti et al. (U.S. 2001/0017770) in view of the capacitor of Young et al. (U.S. Patent No. 4,002,542) and the encapsulation testing method of DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or the thermal head of Nakamura et al. (U.S. Patent No. 5,940,110) in rejecting the method of making the discrete component chip resistor of claims 1-5 as obvious?
2. Did the Examiner improperly combine the thermal head of Minami (U.S. Patent No. 4,777,583) in view of the capacitor of Young et al. (U.S. Patent No. 4,002,542) and the encapsulation testing method of DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or the thermal head of Nakamura et al. (U.S.

Patent No. 5,940,110) in rejecting the method of making the discrete component chip resistor of claims 1-2 as obvious?

3. Did the Examiner improperly combine the thermal head of Minami (U.S. Patent No. 4,777,583) in view of the capacitor of Young et al. (U.S. Patent No. 4,002,542) and the encapsulation testing method of DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or the thermal head of Nakamura et al. (U.S. Patent No. 5,940,110), and further in view of Oki Electric Ind. Co Ltd (Japan 52-3196) in rejecting claims 3-5 as obvious?
4. Did the Examiner improperly combine thermal head of Fuyama et al. (U.S. Patent No. 4,617,575) in view of the encapsulation testing method of DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or the thermal head of Nakamura et al. (U.S. Patent No. 5,940,110), and further in view of the thermal head of Sato (Japan 61-27264) and Oki Electric Ind. Co Ltd (Japan 52-3196) in rejecting claims 15 and 16 as obvious?
5. Did the Examiner improperly combine the multi-component module of Copetti et al. (U.S. 2001/0017770) in view of the thermal head of Fuyama et al. (U.S. Patent No. 4,617,575) and the encapsulation testing method of DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or the thermal head of Nakamura et al. (U.S. Patent No. 5,940,110) in rejecting claims 15 and 16 as obvious?

VII. GROUPING OF THE CLAIMS

For purposes of considerations, claims 1-5 are grouped together and rise and fall together. Claim 15 is not grouped with other claims. Claim 16 is not grouped with other claims. The claims are grouped in this manner as claims 1, 15 and 16 are all independent claims with separate basis for patentability as is evidenced by the fact that the Examiner relies upon different combinations of references in rejecting claims 1-5 and 15 and 16. Claim 15 has an independent reason for patentability than claim 16 as claim 15 requires testing step and includes a passivation layer, the inclusion of the testing step making the prior art cited by the Examiner more remote.

VIII. ARGUMENT

- A. The Examiner improperly relies upon the multi-component module of Copetti et al. in view of the capacitor of Young et al. and the encapsulation testing method of DerMarderosian, Jr. or the thermal head of Nakamura et al. in rejecting the method of making the discrete component chip resistor of claims 1-5 as obvious**

Claims 1-5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Copetti et al. (U.S. 2001/0017770) in view of Young et al. (U.S. Patent No. 4,002,542) and DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or Nakamura et al. (U.S. Patent No. 5,940,110). The Examiner argues that the only differences between Copetti et al. and the present claims is that:

"The differences between the Copetti et al. and the present claims is that depositing the tantalum pentoxide without utilizing oxidation to deposit the film is not discussed, exposing the thin film chip resistors to powered moisture conditions is not discussed and observing failures due to electrolytic

corrosion under powered moisture conditions is not discussed" (Office Action of February 20, 2004, p. 3, lines 10-15).

Then the Examiner attempts to plug the first of these holes by relying upon Young to show depositing of tantalum pentoxide, Young showing a capacitor where tantalum pentoxide is deposited as a dielectric between electrodes of a capacitor. The Examiner's purported motivation or suggestion to combine is that depositing the tantalum pentoxide layer allows for a film with reduced electrical series resistance (Office Action of February 20, 2004, p. 5, lines 3-5).

The Examiner attempts to fill the next gap by relying on DerMarderosian, Jr. which discloses testing of encapsulation with an electrolytic solution. The Examiner's purported motivation or suggestion to combine is that performing testing under powered moisture conditions allows for providing a test that is less costly, more accurate, less time consuming and does not involve the use of hazardous chemicals (Office Action of February 20, 2004, p. 5, line 19-22, citing col. 3, lines 1-5 of DerMarderosian, Jr.).

As an alternative, the Examiner relies upon Nakamura instead of DerMarderosian, Jr.. The Examiner relies upon Nakamura to discloses a test which confirmed that by tapering of an electrode, moisture ions of a thermosensitive paper were prevented from entry in the thermal head in order to prevent corrosion (Office Action of February 20, 2004, p. 6, lines 1-13, citing col. 10, lines 63-68; col. 11, lines 1-14 of Nakamura).

The Examiner's rejection here is improper for a number of reasons. First, the Examiner fails to properly consider each and every limitation in claim 1 and no combination

of the references relied upon by the Examiner disclose each and every limitation of claim 1.

Second, the Examiner fails to consider the invention as a whole, and instead is merely trying to piece together diverse references to support an improper combination.

1. Copetti and Young Disclose Use of a Tantalum Oxide Dielectric to Separate Two Conductors and Do Not Disclose "Depositing an Outer Moisture Barrier of Tantalum Pentoxide."

Copetti and Young only use tantalum pentoxide as a dielectric to separate the conductive layers (or electrodes) of a capacitor. Thus, neither Copetti nor Young disclose "depositing an outer moisture barrier" that consists of tantalum pentoxide as required by claims 1-5. Both Copetti and Young use tantalum pentoxide as a dielectric—to separate conductive layers or electrodes of a capacitor. Thus, neither Copetti nor Young discloses using tantalum pentoxide as an outer layer, let alone an "outer moisture barrier." It is further observed that in addition to this structural difference, the purpose of the tantalum pentoxide as an outer moisture barrier is further made clear as claim 1 further requires the limitation of "wherein the outer moisture barrier reduces failures due to electrolytic corrosion under powered moisture conditions." Because the dielectrics of Copetti and Young serve as dielectrics to separate layers, neither serves to reduce failures due to electrolytic corrosion under powered moisture conditions.

It is further observed that the Examiner does not rely upon any of the remaining references for disclosing "depositing an outer moisture barrier of tantalum pentoxide." Moreover, DerMarderosian, Jr. does not disclose any use of tantalum pentoxide, let alone

"depositing an outer moisture barrier of tantalum pentoxide." Nakamura relates to a thermal head and instead of using a tantalum pentoxide film uses a protective film having a Vickers harness of at least 1200 Kg/mm² or more (abstract). It is further observed that Nakamura teaches away from the use of a tantalum pentoxide as a moisture barrier in a thermal head as Nakamura disclosures that if a protective film made of tantalum pentoxide is used, during printing moisture will enter into the thermal head causing corrosion (Col. 1, lines 22-25; lines 44-51). Thermal head art is not the appropriate art to be considering as the claims are directed towards a discrete component chip resistor, not a thermal head, but to the extent Nakamura is considered, when taken as a whole, Nakamura teaches away from the claims of the present invention.

2. The Examiner Fails to Reasonably Construe the Limitation of "Forming a Plurality of Discrete Component Thin Film Chip Resistors."

It is further observed that the methodology of claim 1 requires "forming a plurality of discrete component thin film chip resistors" and although Copetti discloses a module that can contain a resistor, the modules are not "discrete component thin film resistors" required by claim 1. The fact that the module of Copetti *may include a resistor* does not transform the module of Copetti into a chip resistor. The use of the well known term "chip resistor" makes clear that Copetti is deficient.

None of Young , DerMarderosian, Jr., and Nakamura disclose discrete component chip resistors. Therefore none of these references can remedy the fatal deficiency in Copetti.

As none of these references alone or in combination disclose all the limitations of claims 1-5, these rejections must be withdrawn.

3. The Examiner improperly combines the multi-component module of Copetti et al. with the capacitor of Young et al. and the encapsulation testing method of DerMarderosian, Jr. or the thermal head of Nakamura et al.

The Examiner improperly combines the cited references when there is no proper motivation to do so and in a manner that fails to appreciate the claimed invention as a whole and the problems solved by the Applicant's claimed invention. In making the improper rejections, the Examiner has not properly considered the problem being solved by the applicant's invention which is the corrosion of a chip resistor under powered moisture conditions. The problem being solved is clear from the language of the claims which includes the method steps of "exposing selected thin film chip resistors to powered moisture conditions" and "observing failures due to electrolytic corrosion under powered moisture conditions in the selected thin film chip resistors." As the Federal Circuit has held, "The problem solved by the invention is always relevant." *In re Wright*, 838 F.2d 1216, 6 U.S.P.Q.2d 1959, 1961 (Fed. Cir. 1988). Instead of considering the invention as a whole, the Examiner improperly focuses on the obviousness of substitutions and differences. This is not permitted. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 U.S.P.Q. 81, 93 (Fed. Cir. 1986). For example, the Examiner combines Copetti and Young on the basis that using a tantalum pentoxide layer allows for a film with reduced electrical series resistance (Office Action of February 20, 2004, p. 5, lines 3-5). The electrical series

resistance (ESR) is a measurement associated with capacitors not chip resistors! In other words, the Examiner is combining the capacitors of Young with the capacitors of Copetti in attempts to conjure a rejection that combines two references not on any basis related to the present invention, but on a basis related solely to capacitors, to which the present invention does not pertain. Thus, the Examiner's rejection is inappropriate and must be withdrawn.

B. The Examiner Improperly Relies Upon Minami, Young, and DerMarderosian/Nakamura in Rejecting Claims 1 and 2

Claims 1 and 2 are rejected under U.S.C. § 103(a) as being unpatentable over Minami (U.S. Patent No. 4,777,583) in view of Young et al. (U.S. Patent No. 4,002,542) and DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or Nakamura et al. (U.S. Patent No. 5,940,110). The deficiencies of Young, Nakamura and DerMarderosian, Jr. have already been discussed, as well as the deficiencies in the combination of these references.

Minami is directed towards a thermal head (Title) and not a chip resistor. It is noted that claim 1 explicitly requires forming "discrete component thin film chip resistors." The fact that a thermal head has resistive elements does not make it a "discrete component thin film chip resistor." Therefore this rejection to claim 1 and 2 must be withdrawn as none of the references cited disclose forming a "discrete component thin film chip resistor."

Further, this rejection must be withdrawn because the examiner is relying upon improper motivation. The Examiner's motivation for sputtering tantalum pentoxide is to deposit a film with reduced electrical series resistance (Office Action page 8). As previously

explained, although reduced electrical series resistance is a desirable quality in capacitors (which is what Young is directed towards), it is not a relevant characteristic of the "discrete component thin film chip resistors" of the Applicant's invention. Therefore, the Examiner must be reversed.

C. The Examiner Improperly Combines Minami, Young and DerMarderosian/ Nakamura and Oki in Rejecting Claims 3-5

Claims 3-5 have been rejected under U.S.C. § 103(a) as being unpatentable over Minami et al in view of Young et al., DerMarderosian, Jr. or Nakamura et al. in view of Oki Electric Ind. Co Ltd. Oki Electric teaches that resistance layers can be made from metals such as nichrome. However, for the reasons previously expressed, Minami, DerMarderosian, Jr., and Nakamura are deficient.

As previously expressed, none of these references are directed towards forming a plurality of "discrete component thin film chip resistors." Minami is a thermal head (Title). Nakamura is also directed towards a thermal head (Abstract). DerMarderosian, Jr. is directed towards testing integrated circuits (Abstract). Young is directed towards a capacitor (Abstract). Therefore, the Examiner must be reversed as these references alone or in combination do not disclose each and every element of claim 1. The Examiner relies upon Oki Electric to teach that the resistance layers can be tantalum nitride, NiCr, etc. This does not cure the failure of the previously cited prior art to disclose all of the elements of claim 1. Therefore, as claims 3-5 depend from claim 1, and none of the references alone or in combination disclose each and every limitation of claim 1, these rejections must be reversed.

**D. The Examiner Improperly Relied Upon Fuyama, DerMarderosian/
Nakamura, Sato and OKI in Rejecting Claims 15 and 16.**

Claims 15 and 16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fuyama et al. (U.S. Patent No. 4,617,575) in view of DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or Nakamura et al. (U.S. Patent No. 5,940,110), and further in view of Sato (Japan 61-27264) and Oki Electric Ind. Co Ltd (Japan 52-3196). Fuyama and Sato are directed towards a thermal head, and not to "discrete component thin film chip resistors." The deficiencies of DerMarderosian, Jr., Nakamura, and Oki Electric have already been discussed. As none of the references are directed towards manufacturing discrete component thin film chip resistors the rejection must be reversed as no combination of these references disclose manufacturing discrete component thin film chip resistors, let alone discrete component thin film chip resistors with moisture barriers.

**E. The Examiner Improperly Relied Upon Copetti, Fuyama, and
DerMarderosian/Nakamura in rejecting Claims 15.**

Claims 15 and 16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable under Copetti et al. (U.S. 2001/0017770) in view of Fuyama et al. (U.S. Patent No. 4,617,575) and DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or Nakamura et al. (U.S. Patent No. 5,940,110). The deficiencies of Copetti have already been discussed. In particular, Copetti is directed towards a module and not towards a discrete component thin film chip resistor. Further Copetti does not teach that tantalum pentoxide can be used as a

moisture barrier. The deficiencies of the thermal head disclosure of Fuyama and Nakamura has already been disclosed. Claims 15 is directed towards a method of manufacturing discrete component thin film chip resistors. None of the references cited disclose manufacturing discrete component thin film chip resistors let alone discrete component thin film chip resistors with moisture barriers. Therefore, the Examiner must be reversed.

F. The Examiner Improperly Relied Upon Copetti, Fuyama, and DerMarderosian/Nakamura in rejecting Claim 16.

Claims 16 has been rejected under 35 U.S.C. § 103(a) as being unpatentable under Copetti et al. (U.S. 2001/0017770) in view of Fuyama et al. (U.S. Patent No. 4,617,575) and DerMarderosian, Jr. (U.S. Patent No. 5,076,906) or Nakamura et al. (U.S. Patent No. 5,940,110). The deficiencies of Copetti have already been discussed. In particular, Copetti is directed towards a module and not towards a discrete component thin film chip resistor. Further Copetti does not teach that tantalum pentoxide can be used as a moisture barrier. The deficiencies of the thermal head disclosure of Fuyama and Nakamura has already been disclosed. Claims 15 is directed towards a method of manufacturing discrete component thin film chip resistors. None of the references cited disclose manufacturing discrete component thin film chip resistors let alone discrete component thin film chip resistors with moisture barriers. Therefore, the Examiner must be reversed.

IX. CONCLUSION

For the above-stated reasons, it is submitted that claims 1-5 and 15-16 are in condition for allowance. The decision of the Examiner, therefore, should be reversed and these claims should be allowed.

Enclosed herein please find the Appeal Brief in triplicate and the fee for filing the Appeal in the amount of \$330. Please also consider is a two-month extension of time and included is the fee for the extension in the amount of \$420. Therefore enclosed is our draft in the amount of \$750.00 for these fees. If this amount is not correct, please consider this a request to debit or credit Deposit Account No. 26-0084 accordingly.

Respectfully submitted,

A handwritten signature in cursive script that reads "John D. Goodhue". The signature is written in dark ink and is positioned above a horizontal line.

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APPENDIX

Claim 1 (Previously presented): A method of manufacturing thin film resistors comprising:

forming a plurality of discrete component thin film chip resistors, each of the plurality

formed by:

- (a) depositing a non-tantalum metal film resistive layer on a thin film resistor substrate;
- (b) attaching a thin film resistor termination on each end of the metal film resistive layer; and
- (c) depositing an outer moisture barrier consisting of tantalum pentoxide directly overlaying and contacting the metal film resistive layer to form one of the plurality of thin film chip resistors wherein the moisture barrier is formed from deposition of the tantalum pentoxide and not through oxidation of tantalum and wherein the outer moisture barrier reduces failures due to electrolytic corrosion under powered moisture conditions;

exposing selected thin film chip resistors to powered moisture conditions;

observing failures due to electrolytic corrosion under powered moisture conditions in the selected thin film chip resistors.

Claim 2 (Original): The method of claim 1 wherein the step of depositing a layer of tantalum pentoxide is sputtering tantalum pentoxide film.

Claim 3 (Original): The method of claim 1 wherein the metal film layer is an alloy containing nickel.

Claim 4 (Original): The method of claim 1 wherein the metal film layer is an alloy containing chromium.

Claim 5 (Original): The method of claim 1 wherein the metal film layer is a nickel-chromium alloy.

Claims 6-14 (Canceled).

Claim 15 (Previously presented): A method of manufacturing [[a]] thin film chip resistors comprising:

forming a plurality of discrete component thin film chip resistors, each of the plurality formed by:

- (a) depositing a non-tantalum metal film resistive layer on a substrate;
- (b) attaching a termination on each end of the metal film resistive layer;
- (c) depositing a passivation layer directly overlaying and contacting the metal film layer; and
- (d) depositing an outer moisture barrier consisting of tantalum pentoxide directly overlaying and contacting the passivation layer to form one of the plurality of thin film chip resistors, wherein the moisture barrier is formed from deposition of the tantalum pentoxide and not through oxidation of tantalum;

exposing selected thin film chip resistors from the plurality of thin film chip resistors to
powered moisture conditions;
observing failure due to electrolytic corrosion under powered moisture conditions in the
selected thin film chip resistors.

Claim 16 (Previously presented): A method of manufacturing a discrete component thin
film chip resistor, comprising:
depositing a non-tantalum metal film resistive element on a thin film resistor substrate;
attaching a thin film resistor termination on each end of the non-tantalum metal film resistive
element;
depositing an outer moisture barrier consisting of tantalum pentoxide directly overlaying and
contacting the non-tantalum metal film resistive element;
wherein the moisture barrier is formed from deposition of the tantalum pentoxide and not
through oxidation of tantalum;
wherein the outer moisture barrier reduces failures due to electrolytic corrosion under
powered moisture conditions.